

# Foundation Verilog



Centre for Advanced Studies in Telecommunication (CAST)  
COMSATS Institute of Information Technology



## About the Instructor

Dr. Syed Waqar Nabi completed his Engineering Doctorate in Reconfigurable System-on-Chip design from Edinburgh University, and has also worked at And-Or logic, Islamabad. He is currently heading the Design Methodologies and Rapid Prototyping group at CAST.

## Brief Outline of Contents:

### Session 1:

Introduction to digital IC design, language-based design and HDLs, design abstractions.

### Session 2:

Modules and ports, primitives and gate-level modeling, test-bench, data types, hierarchy.

### Session 3:

Simulation control, Behavioral Modeling using continuous assignments, Procedural blocks for combinational logic

### Session 4:

Time-based and event-based control, synchronous sequential logic, blocking and non-blocking assignments, tasks and functions

### Session 5:

Conditional statements, loops, modeling muxes, encoders/decoders.

### Session 6:

Modeling finite-state machines, modeling counters, shift registers, register files.

## Foundation Verilog

This is a 2-day training workshop on the Verilog® Hardware Description Language. Verilog is a 'Hardware Design Language' or HDL that is used to simulate and model digital hardware. It can be used to design either ASIC or FPGA-based solutions. The workshop targets beginners, and will be composed of lectures and hands-on labs sessions. The syllabus covers the basics of Verilog language, and focuses on coding for Register Transfer Level (RTL) synthesis. Development of test fixtures and use of Verilog tools will also be taught. Students will learn how Verilog fits into the FPGA/ASIC design flow, how to use the Verilog language for hardware design and logic synthesis, how to write Verilog test fixtures to verify your designs, and how to code Verilog for synthesis.

## CAST

CAST has been developed to bridge university-based telecommunication activities and regional telecom industry under the auspice of COMSATS Institute of Information Technology. The mission of CAST is to provide a prominent service

## Program Schedule

<b>Duration:</b>	<b>02 day</b>
<b>Timings:</b>	<b>1000 - 1700hrs</b>
<b>Dates:</b>	<b>Dec 26-27, 2009</b>
<b>Workshop Fees:</b>	<b>Rs. 1,500/-</b>

**Last Date of Registration:**  
**December 23rd, 2009**

to society by promoting quality research in telecommunication by virtue of its highly competent researchers, state-of-the-art research facilities, and mutual relationship with regional industry and by providing an intellectually stimulating environment for post-graduate studies.

## Who Should Attend

The workshop is primarily aimed at students, graduate and undergraduate, but anyone interested in getting hands-on with Verilog is welcome to attend. The workshop will be ideal for students planning an undergraduate or graduate project involving Digital Hardware Design.

## Pre-Requisites

- Background in basic digital logic design, typically taught to CS and EE undergraduate students.
- Programming background in any language is recommended.

## For Registration and Information

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